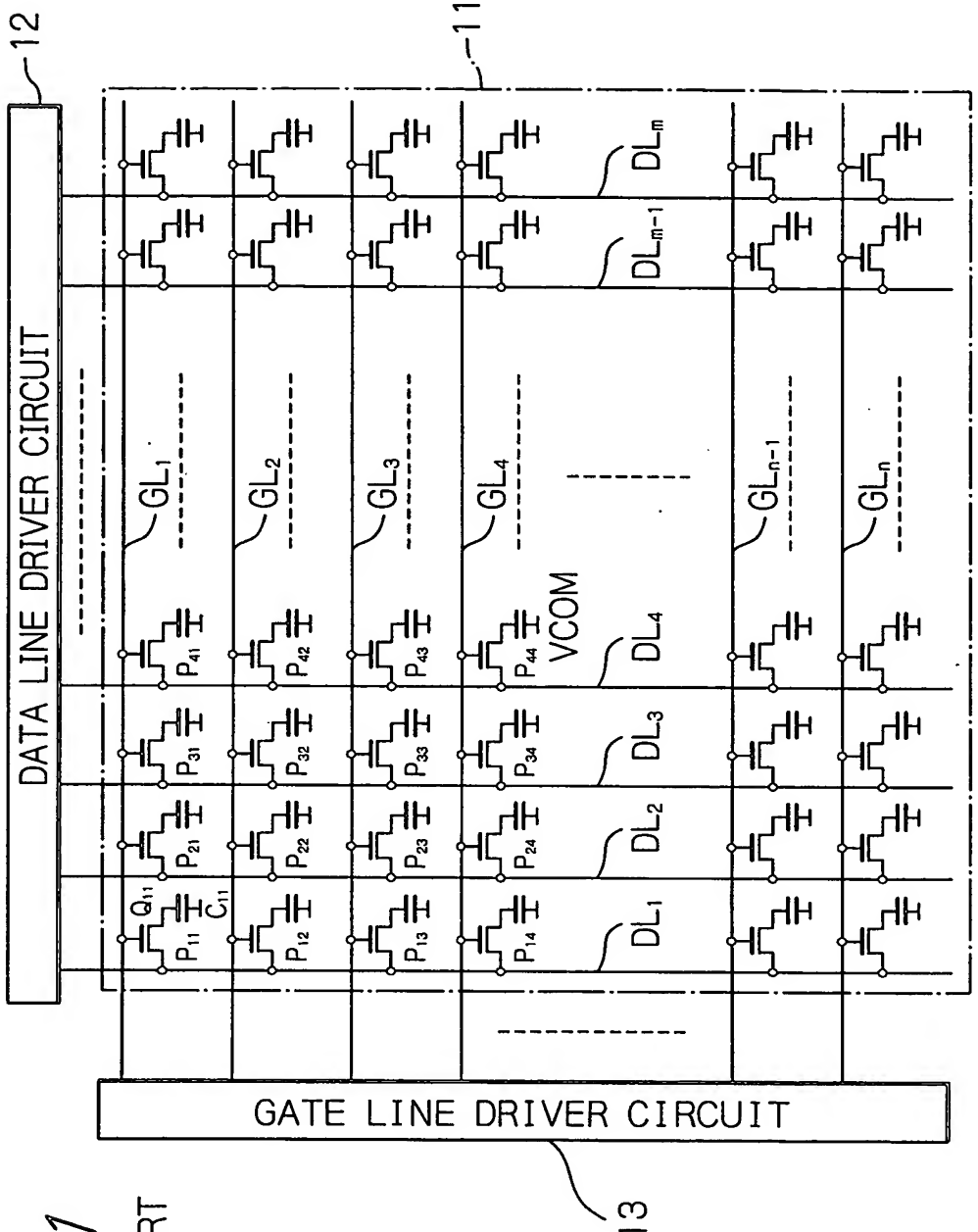
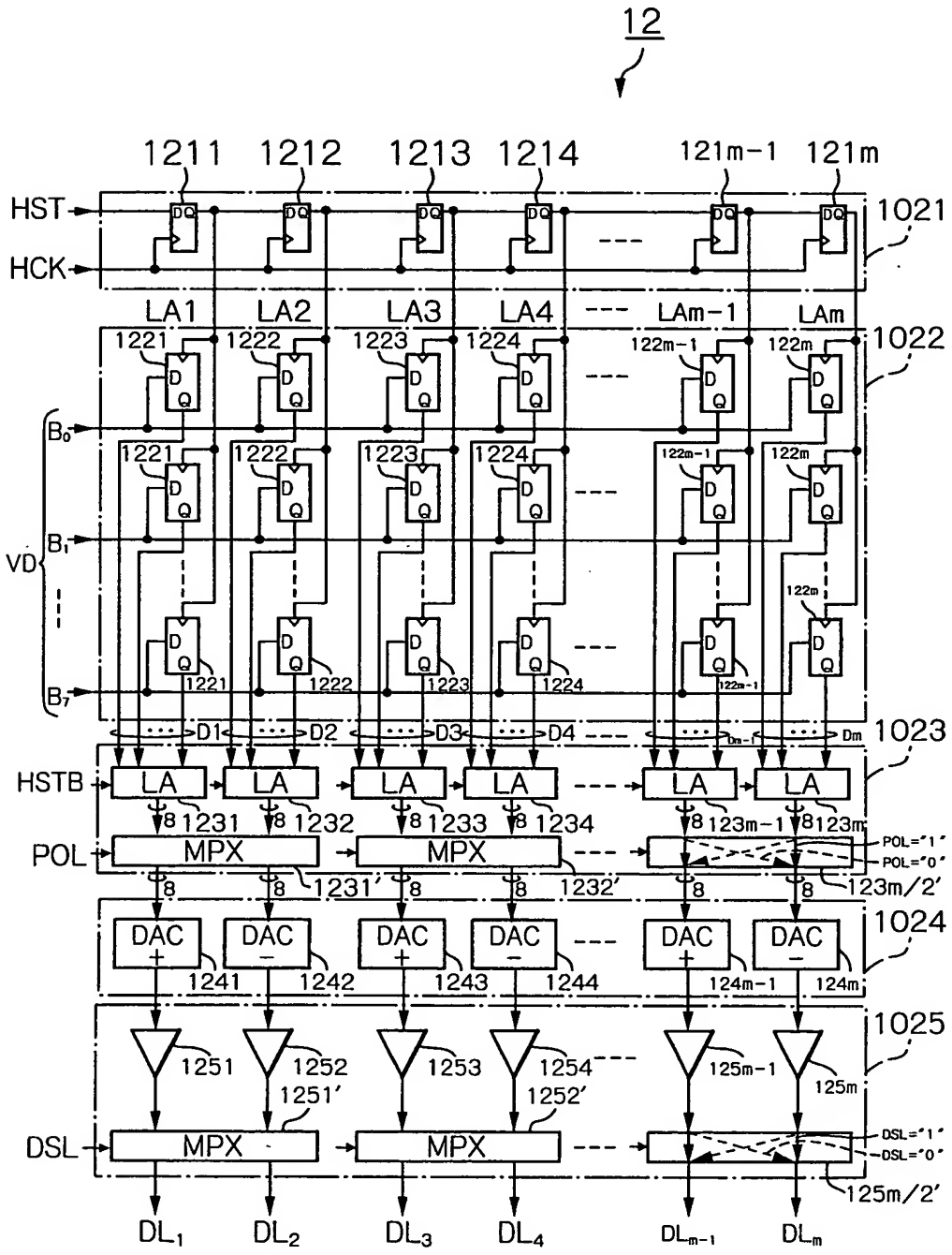


Fig. 1
PRIOR ART

Fig. 2 PRIOR ART



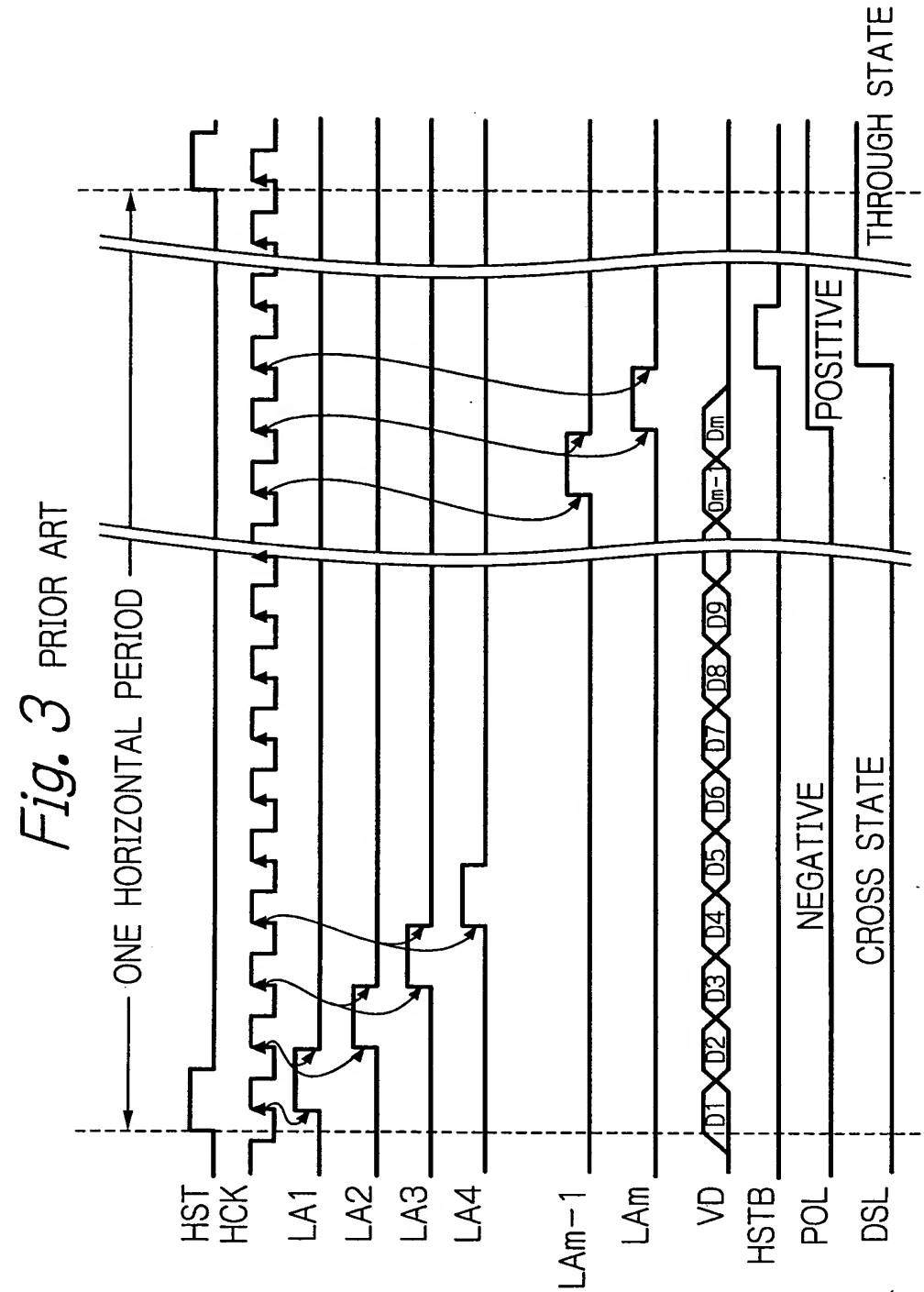
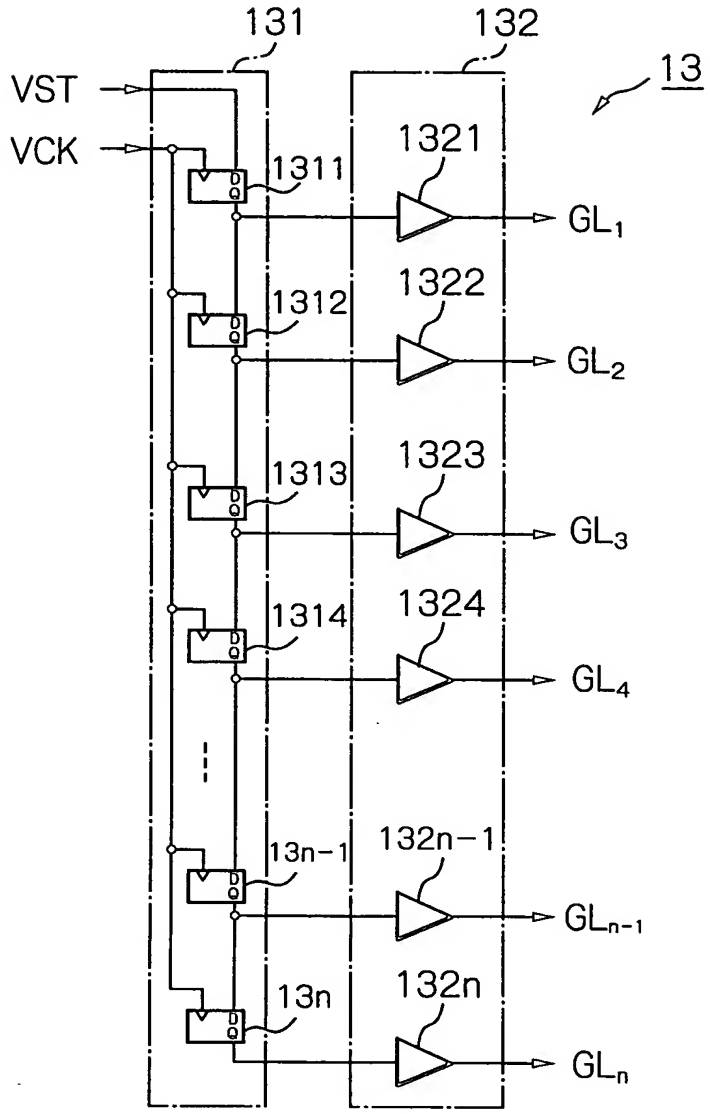


Fig. 3 PRIOR ART

Fig. 4 PRIOR ART



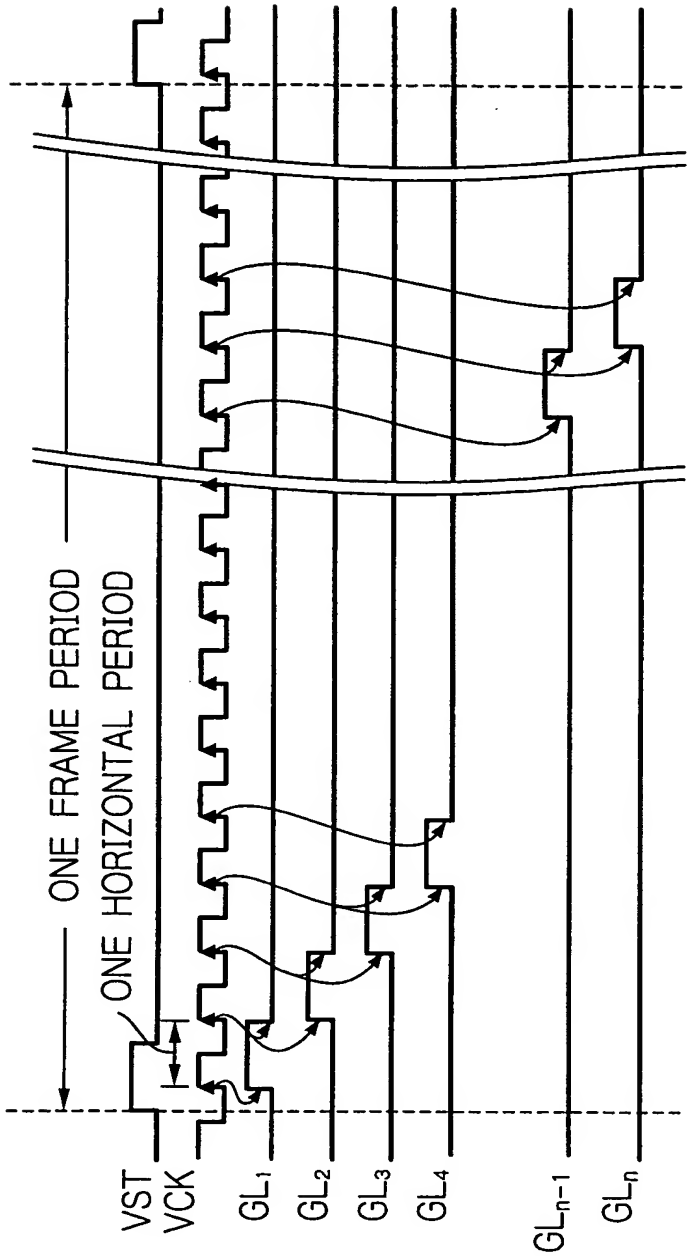
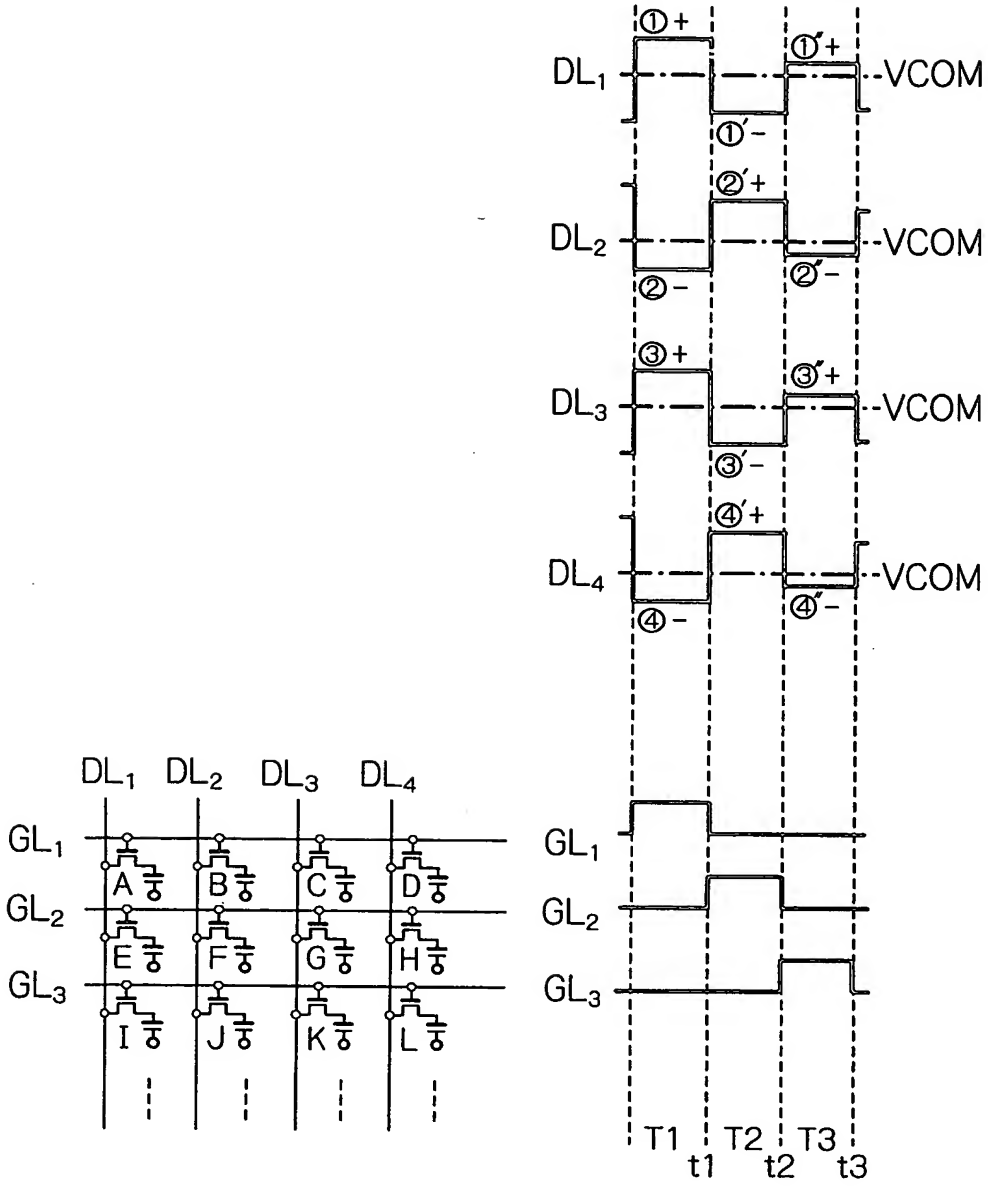


Fig. 5 PRIOR ART

Fig. 6 PRIOR ART



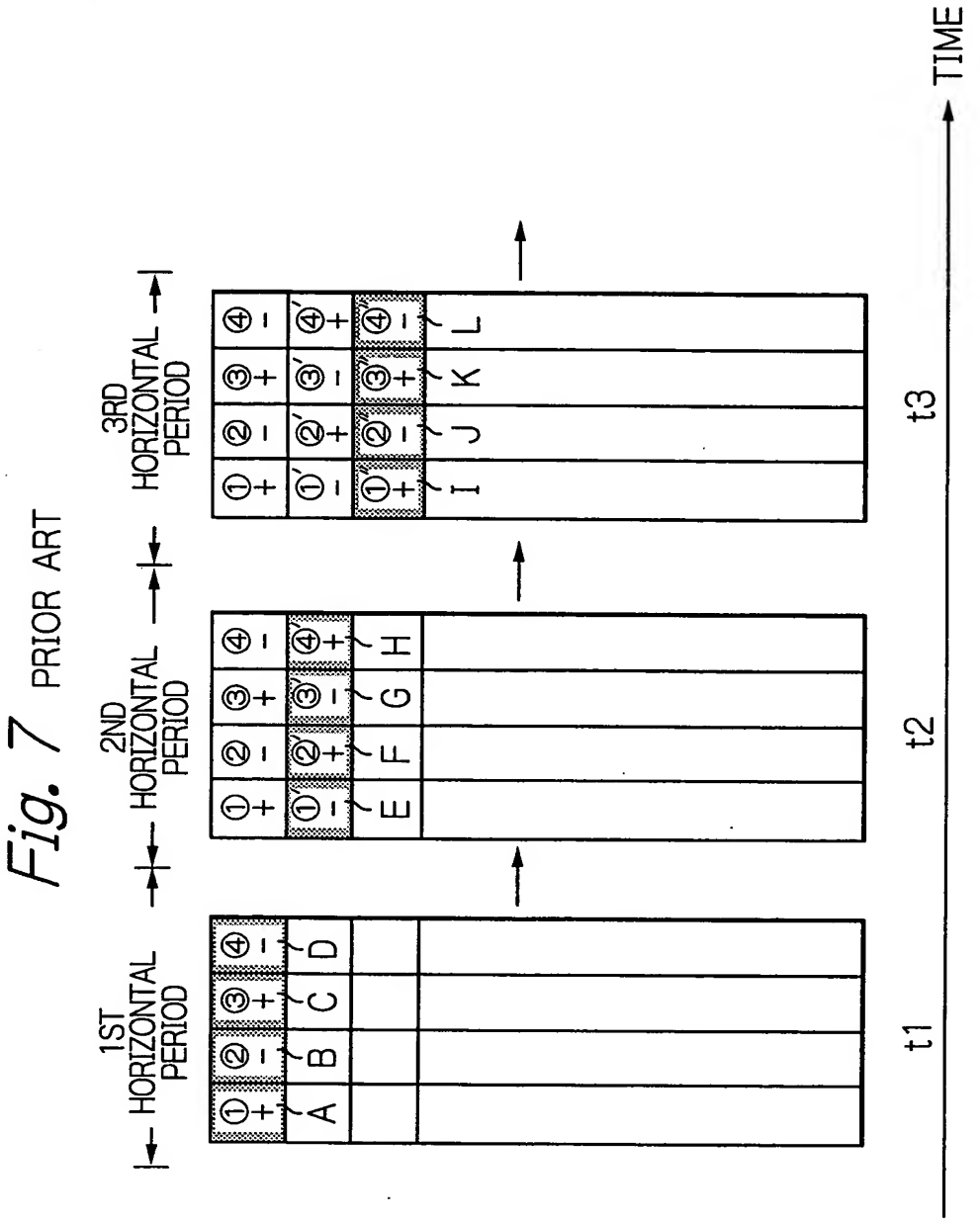


Fig. 7 PRIOR ART

Fig. 8 PRIOR ART

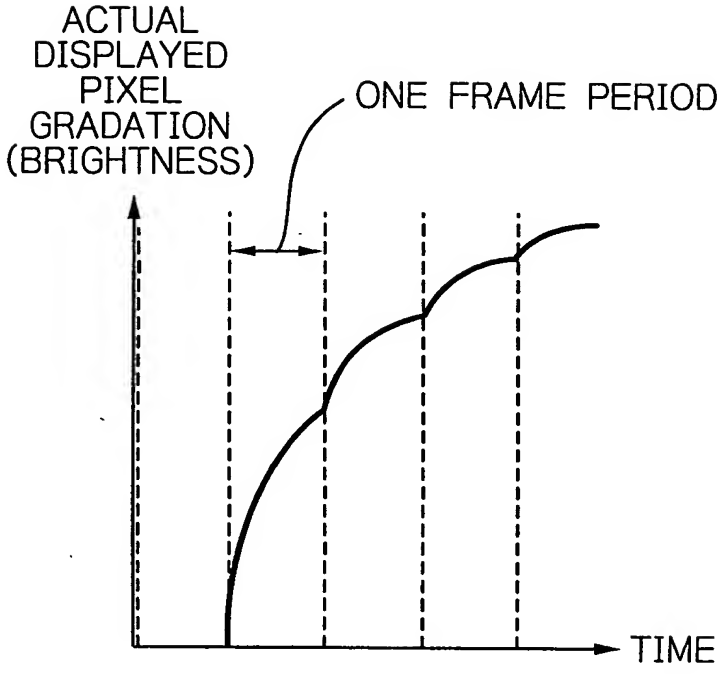


Fig. 9A PRIOR ART

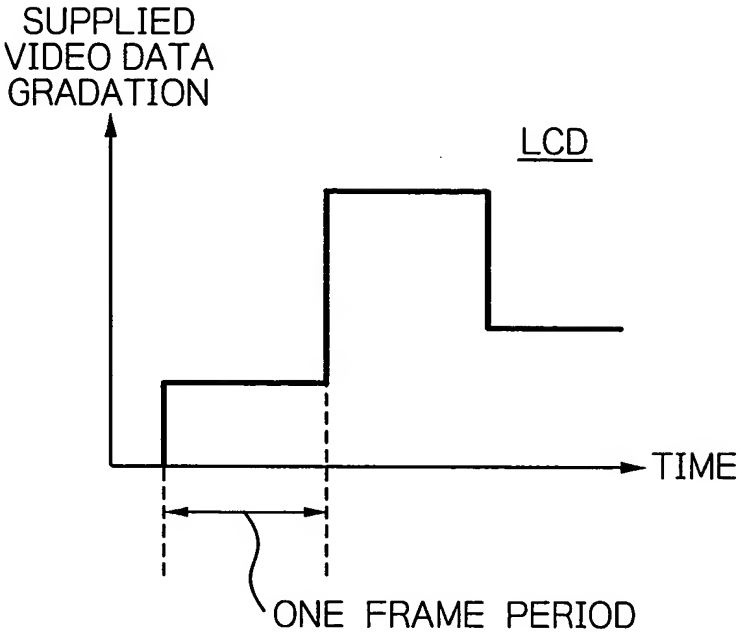
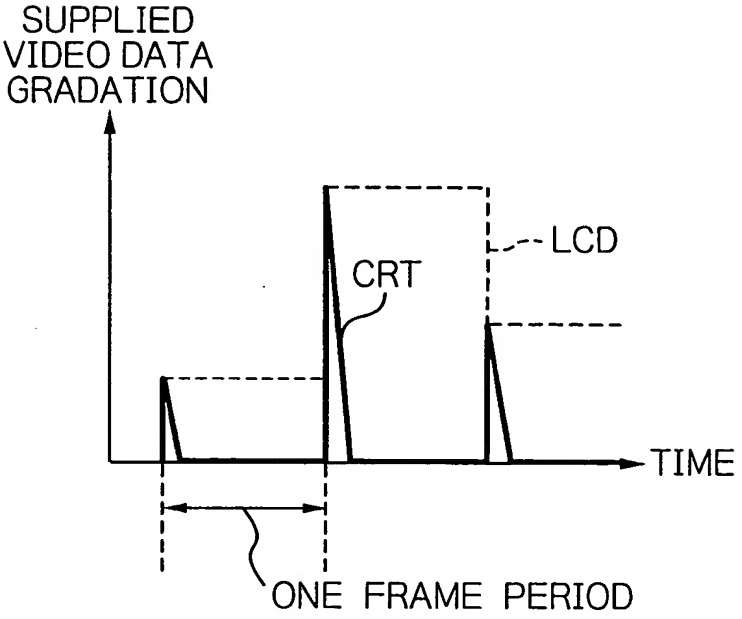


Fig. 9B PRIOR ART



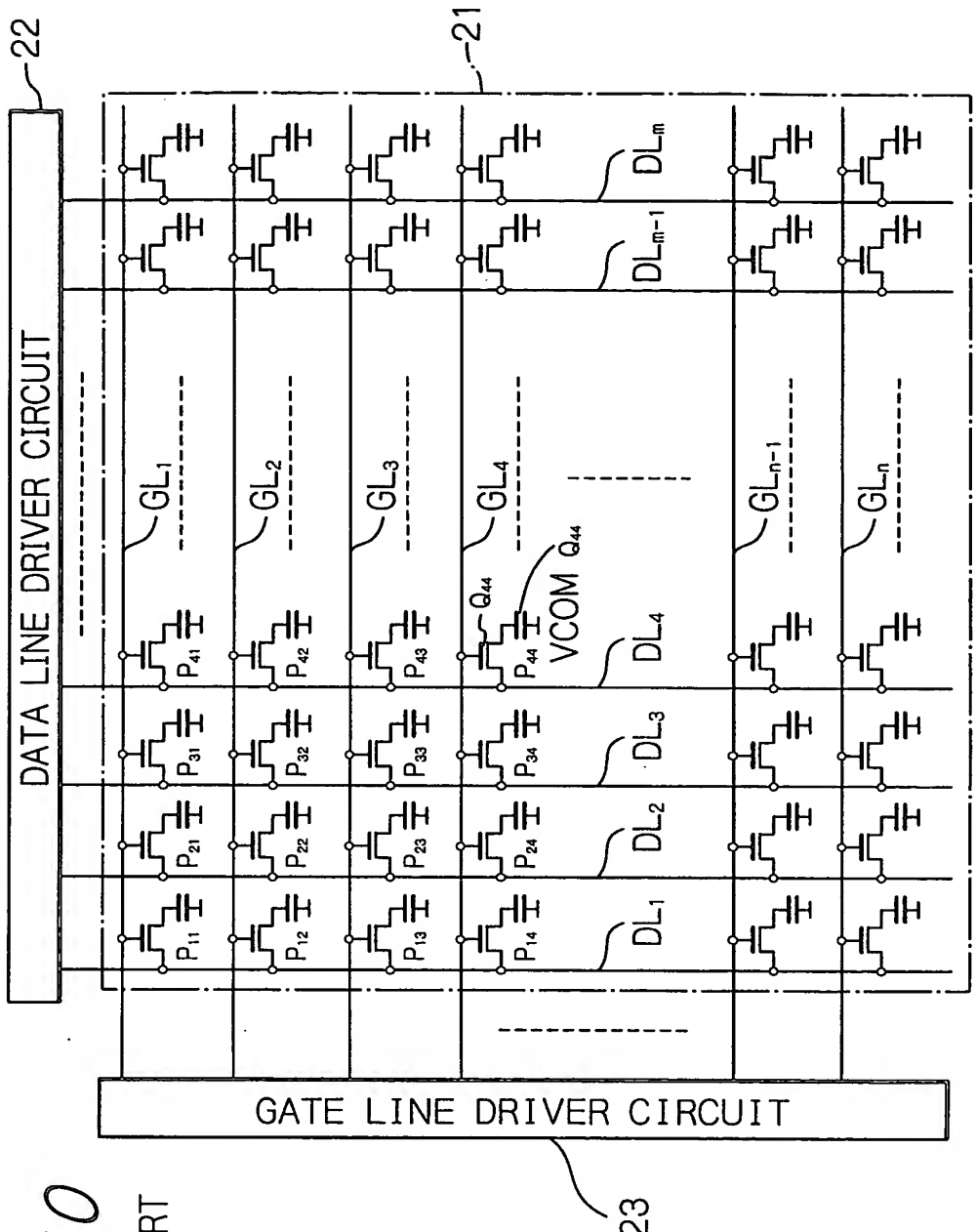
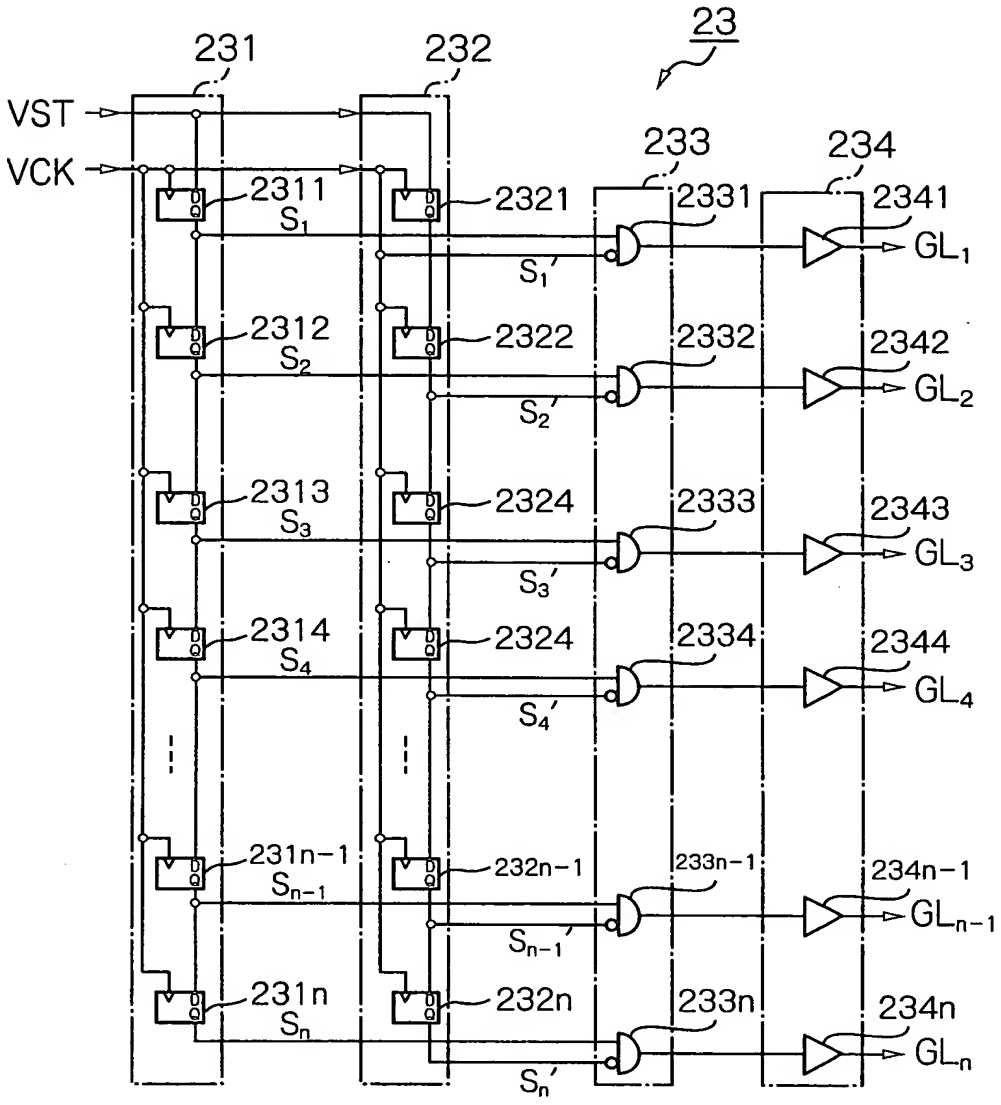


Fig. 10
PRIOR ART

Fig. 11 PRIOR ART



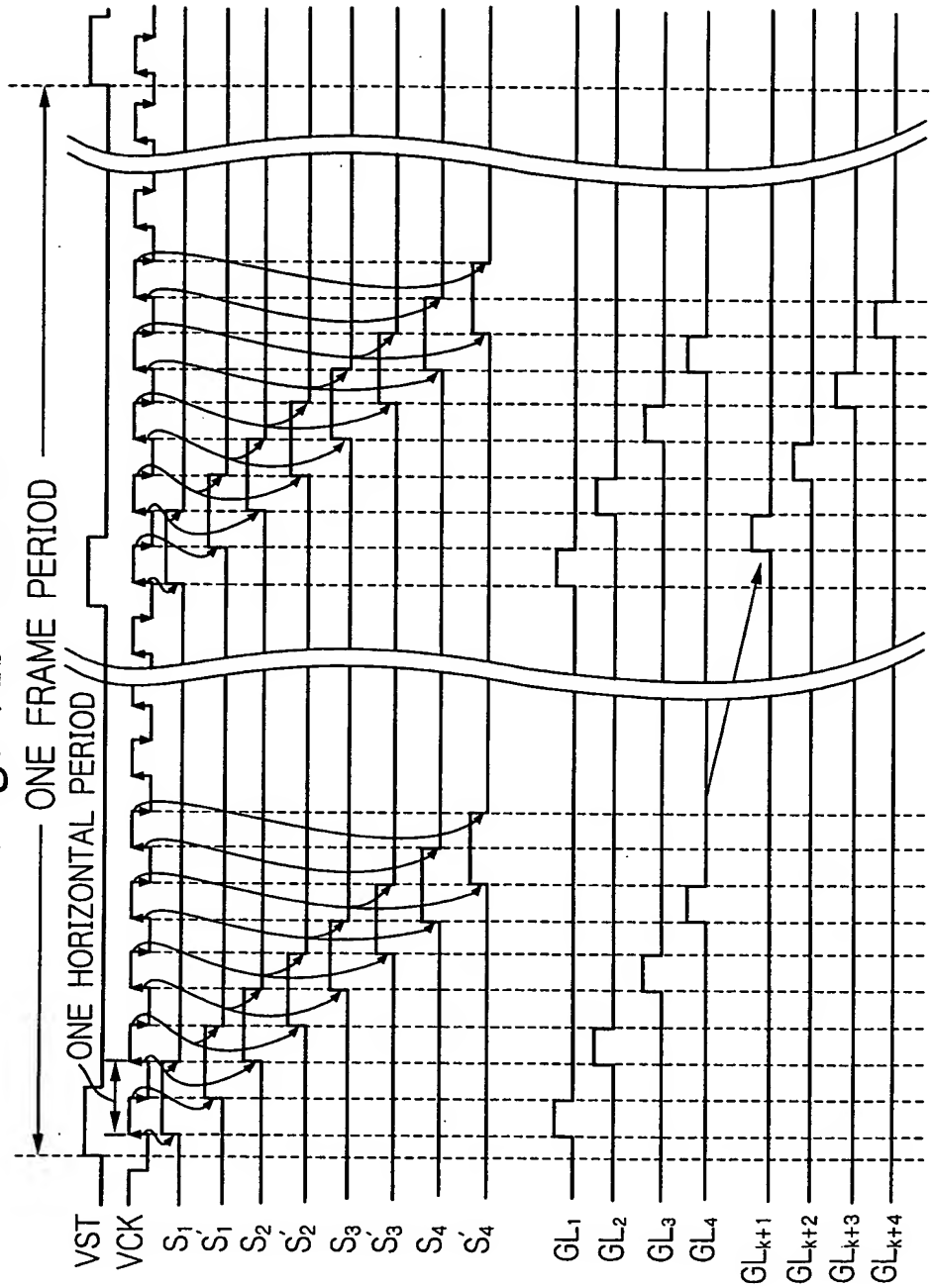


Fig. 12 PRIOR ART

Fig. 13

PRIOR ART

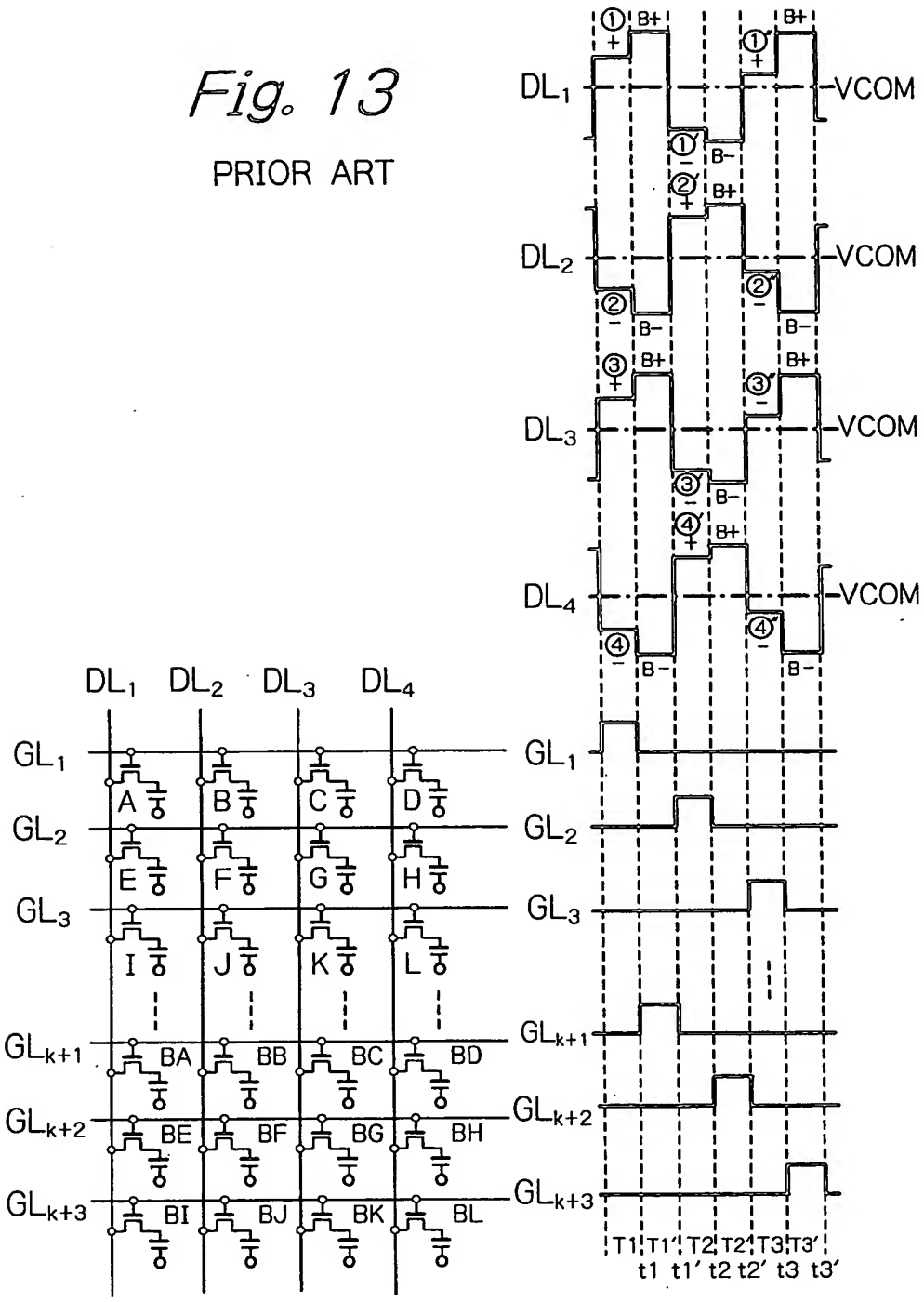


Fig. 14 PRIOR ART

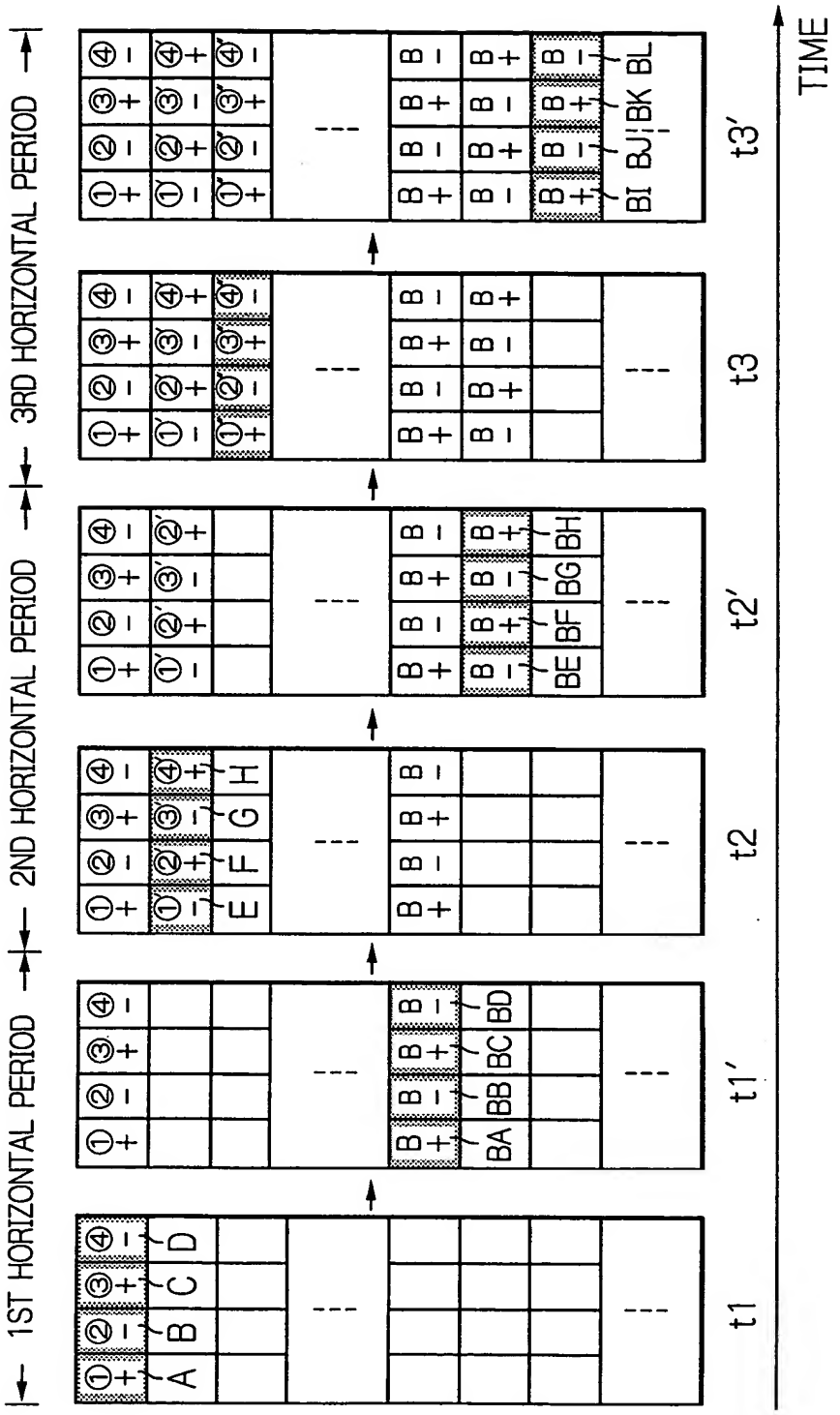
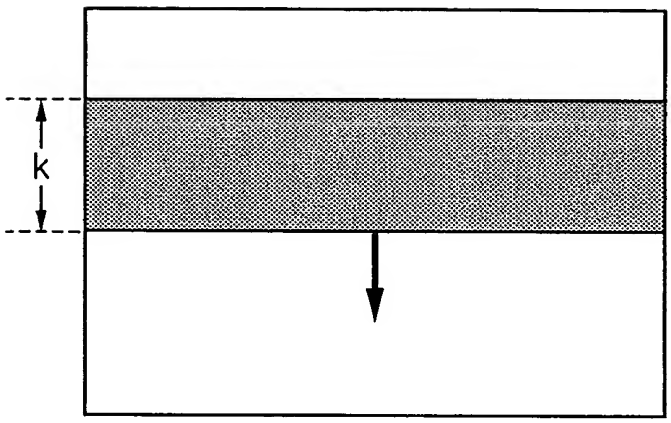


Fig. 15 PRIOR ART



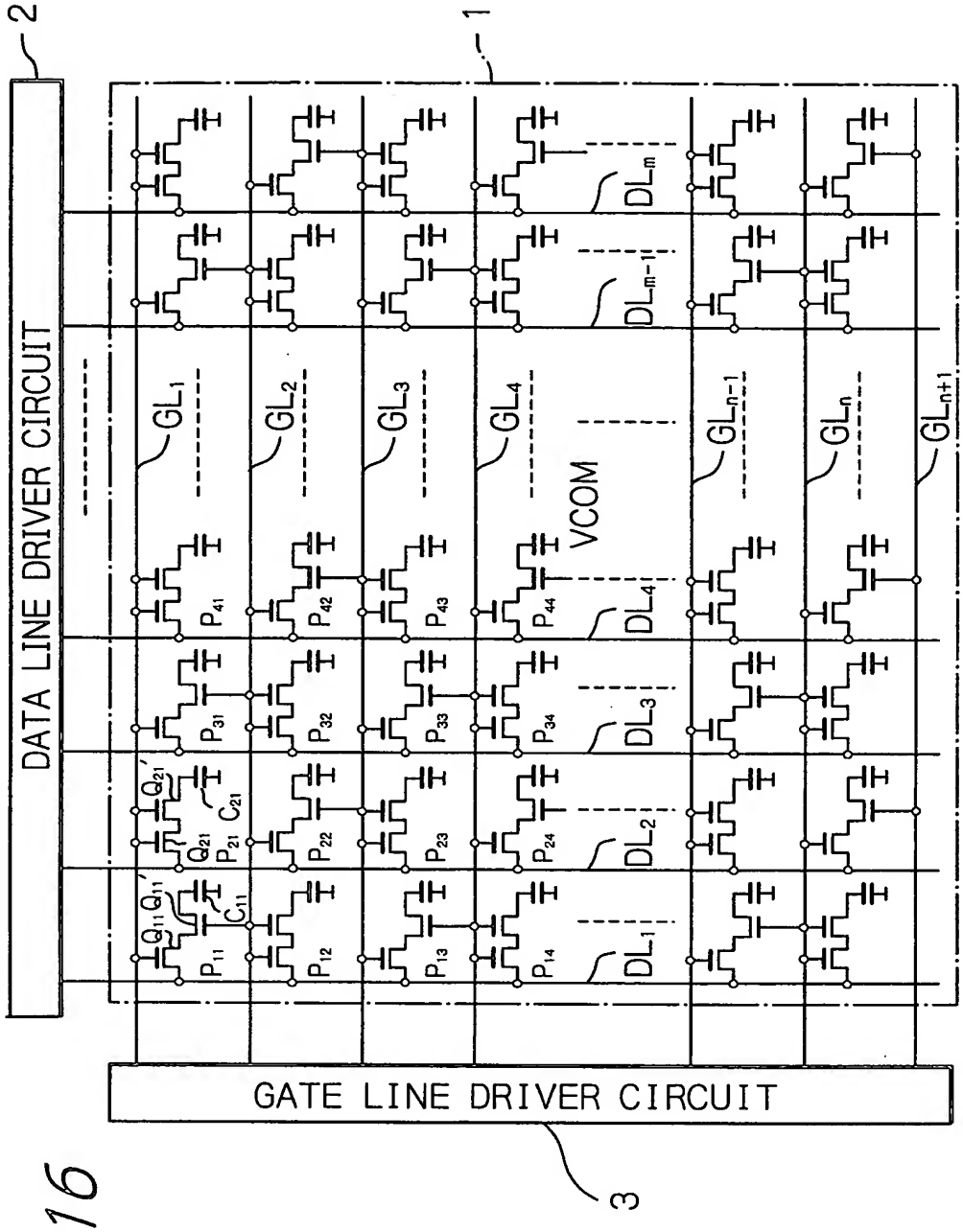

2
1
DATA LINE DRIVER CIRCUIT
GL1
GL2
GL3
GL4
VCOM
GLn-1
GLn
GLn+1
DLm
DLm-1
DL4
DL3
DL2
DL1
P41
P42
P43
P44
P31
P32
P33
P34
P21
P22
P23
P24
P11
P12
P13
P14
Q21'
Q21
C21
Q11'
Q11
C11
GATE LINE DRIVER CIRCUIT
3

Fig. 16

Fig. 17

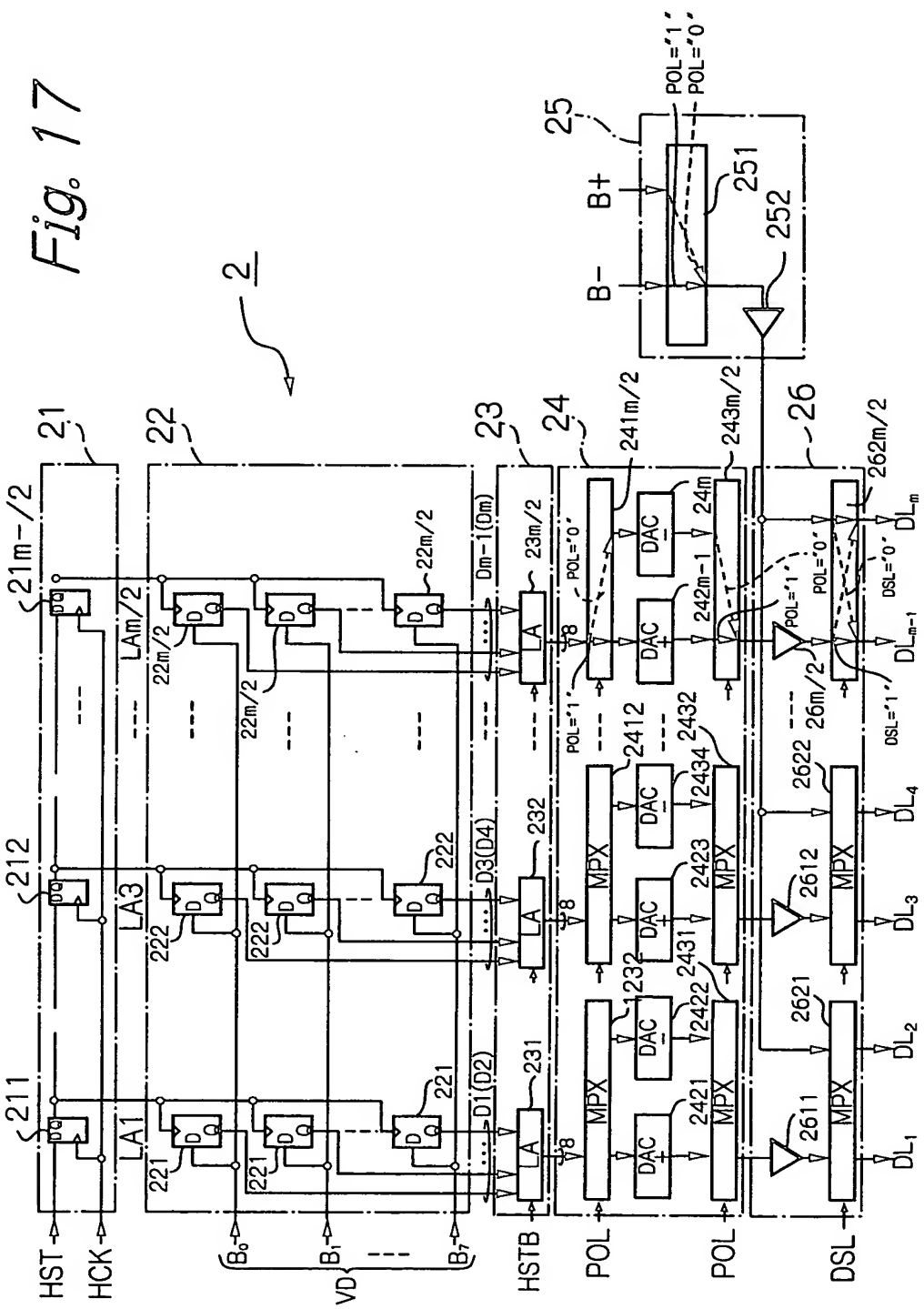
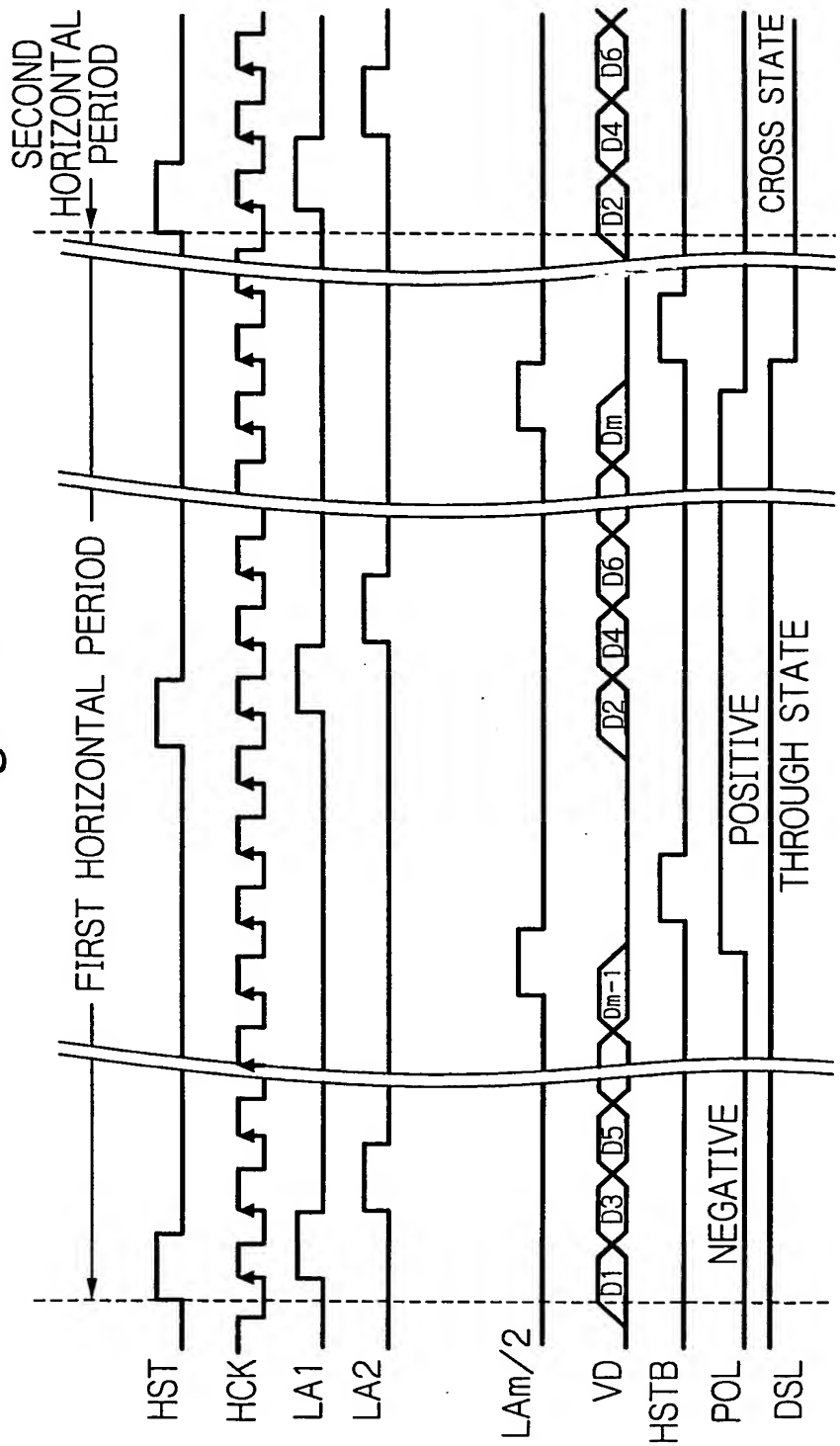

2
21
22
23
24
25
26
HST
HCK
HSTB
POL
DSL
VD
B+
B-
POL="1"
POL="0"
DSL="1"
DSL="0"
MPX
DAC
LA
LA1
LA3
LAm/2
D1(D2)
D3(D4)
Dm-1(Dm)
211
212
21m-/2
221
222
231
232
241m/2
242m-1
243m/2
251
252
262m/2
2412
2423
2434
2432
2611
2612
2621
2622
DL1
DL2
DL3
DL4
DLm-1
DLm

Fig. 18


FIRST HORIZONTAL PERIOD
SECOND HORIZONTAL PERIOD
HST
HCK
LA1
LA2
LAm/2
VD
HSTB
POL
DSL
D1
D3
D5
Dm-1
D2
D4
D6
Dm
NEGATIVE
POSITIVE
THROUGH STATE
CROSS STATE

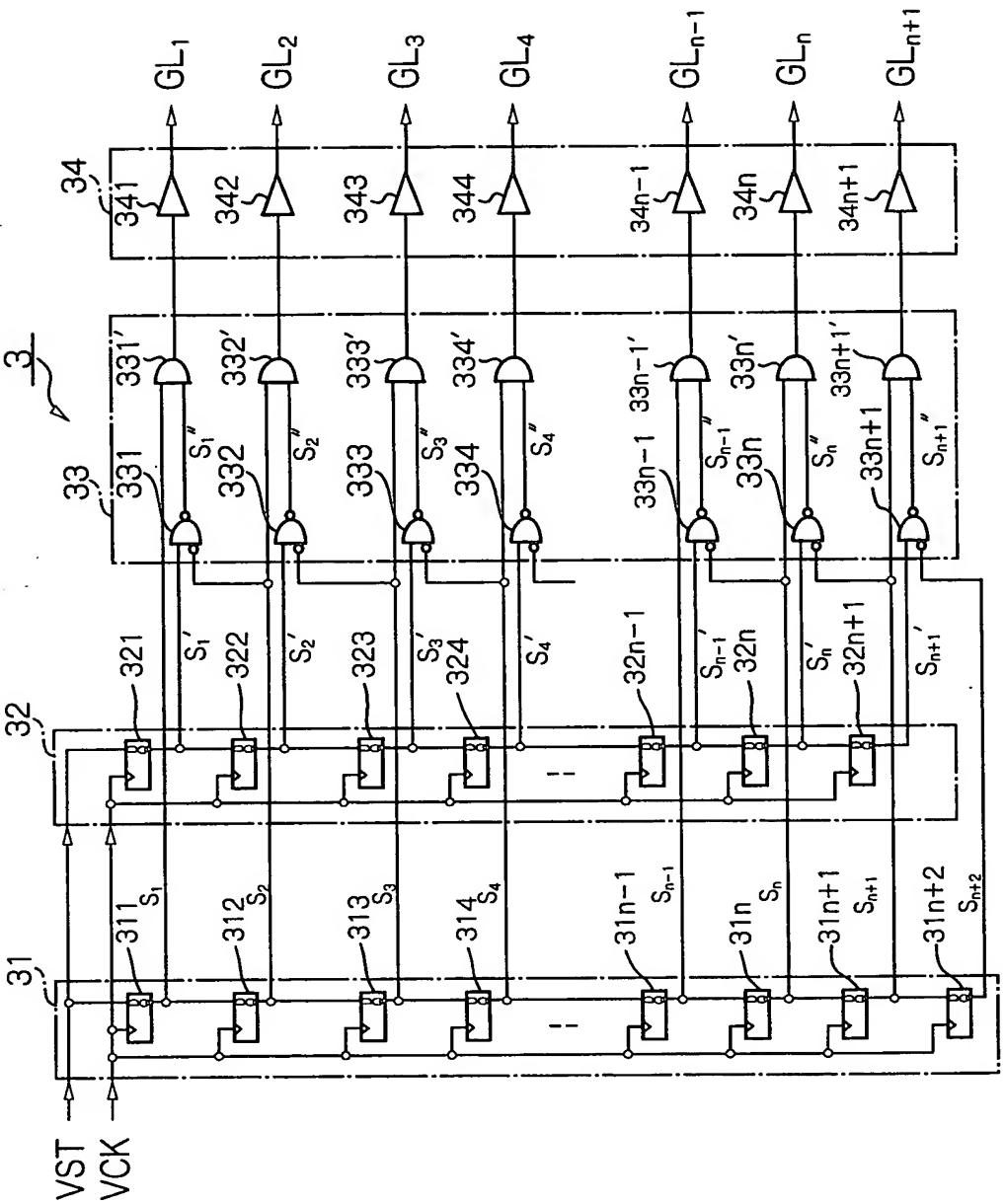

VST
VCK
31
32
33
34
3
311
312
313
314
31n-1
31n
31n+1
31n+2
321
322
323
324
32n-1
32n
32n+1
331
332
333
334
33n-1
33n
33n+1
331'
332'
333'
334'
33n-1'
33n'
33n+1'
341
342
343
344
34n-1
34n
34n+1
GL1
GL2
GL3
GL4
GLn-1
GLn
GLn+1

Fig. 19

Fig. 20

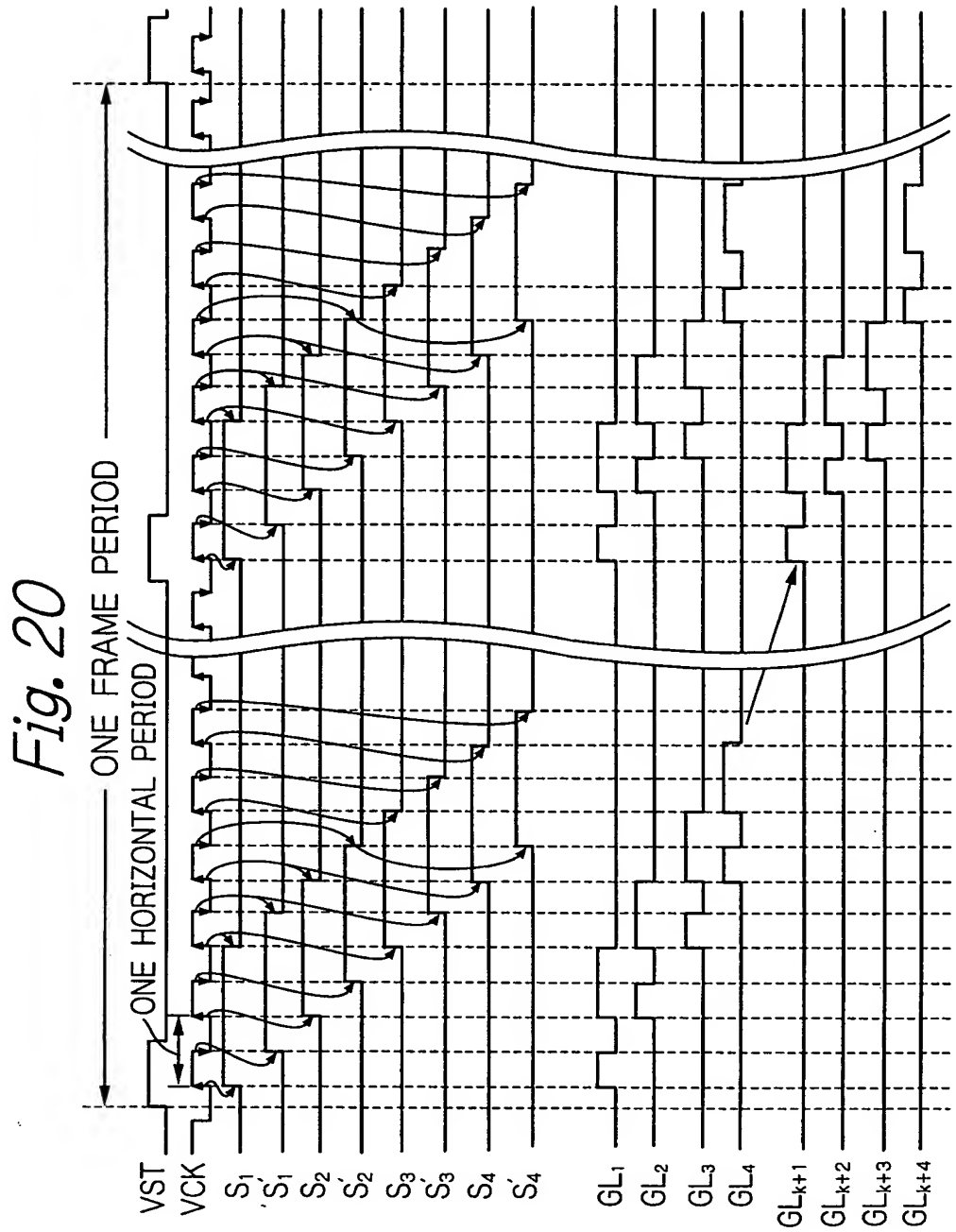

ONE FRAME PERIOD
ONE HORIZONTAL PERIOD
VST
VCK
S1
S'1
S2
S'2
S3
S'3
S4
S'4
GL1
GL2
GL3
GL4
GLk+1
GLk+2
GLk+3
GLk+4

Fig. 21

"HZ"=high impedance

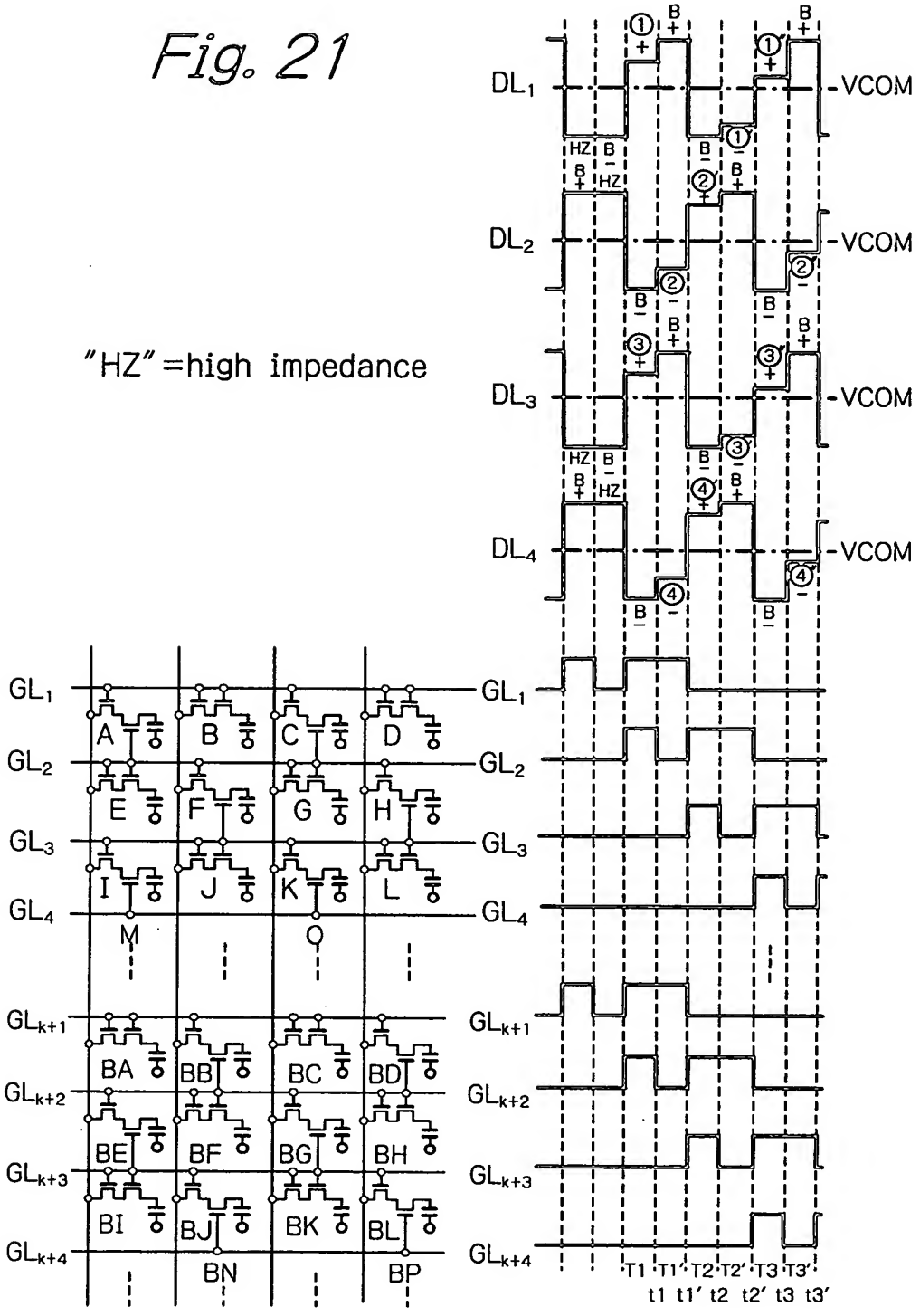
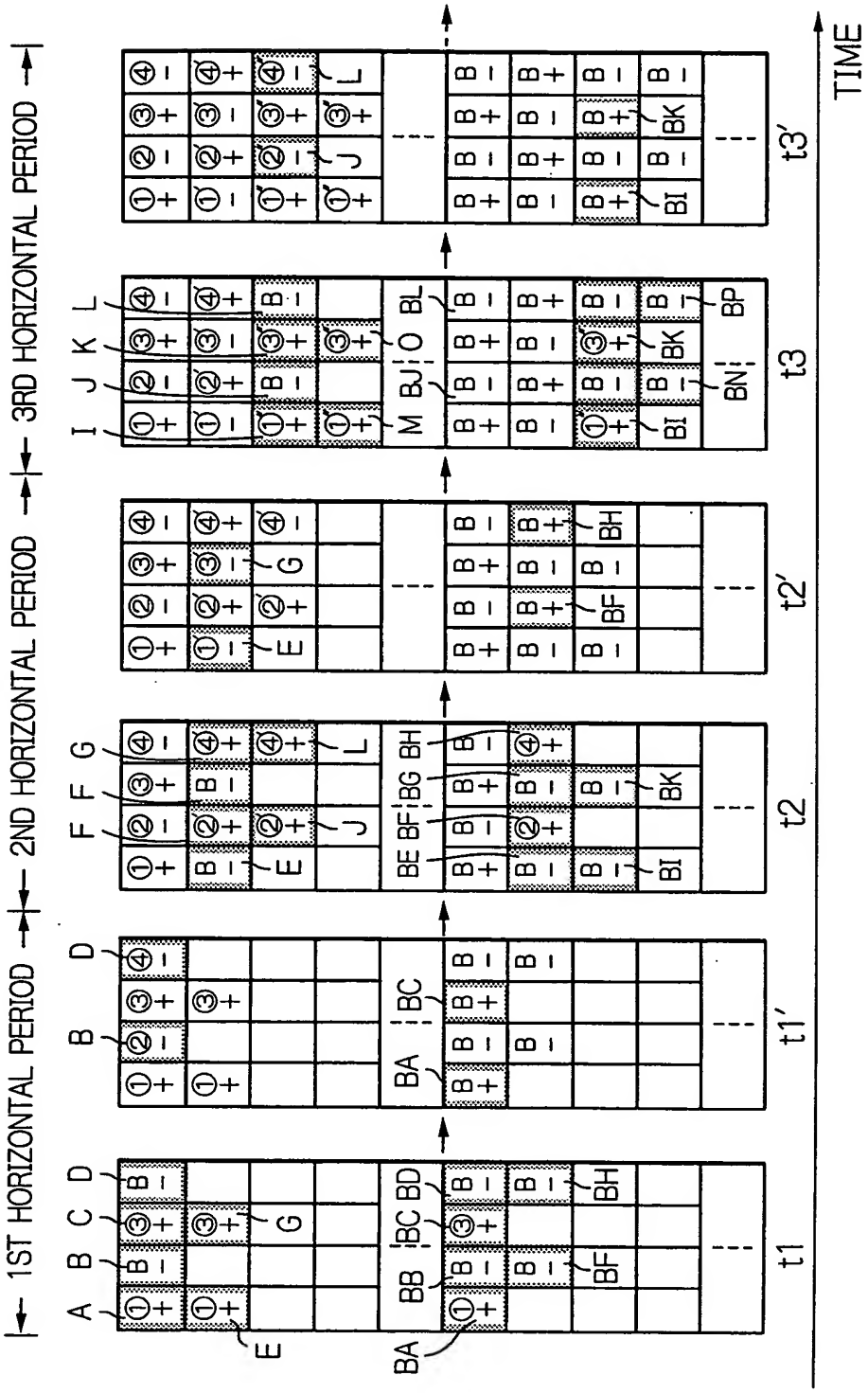


Fig. 22


1ST HORIZONTAL PERIOD
2ND HORIZONTAL PERIOD
3RD HORIZONTAL PERIOD
TIME
t1
t1'
t2
t2'
t3
t3'

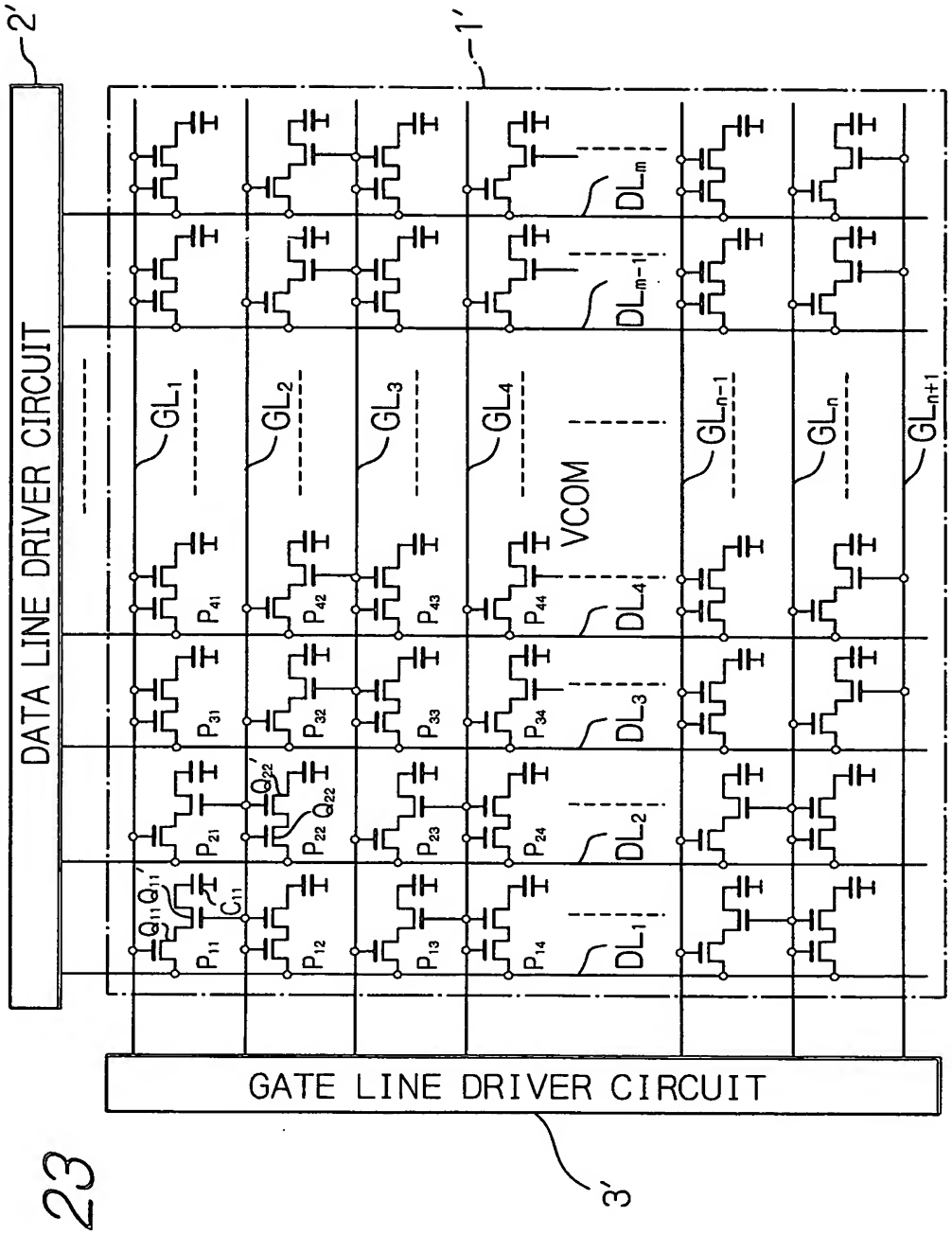

2'
1'
DATA LINE DRIVER CIRCUIT
GL1
GL2
GL3
GL4
VCOM
GLn-1
GLn
GLn+1
DLm
DLm-1
DL4
DL3
DL2
DL1
P41
P42
P43
P44
P31
P32
P33
P34
P21
P22
P23
P24
P11
P12
P13
P14
Q22'
Q22
Q11'
Q11
C11
GATE LINE DRIVER CIRCUIT
3'

Fig. 23

Fig. 24

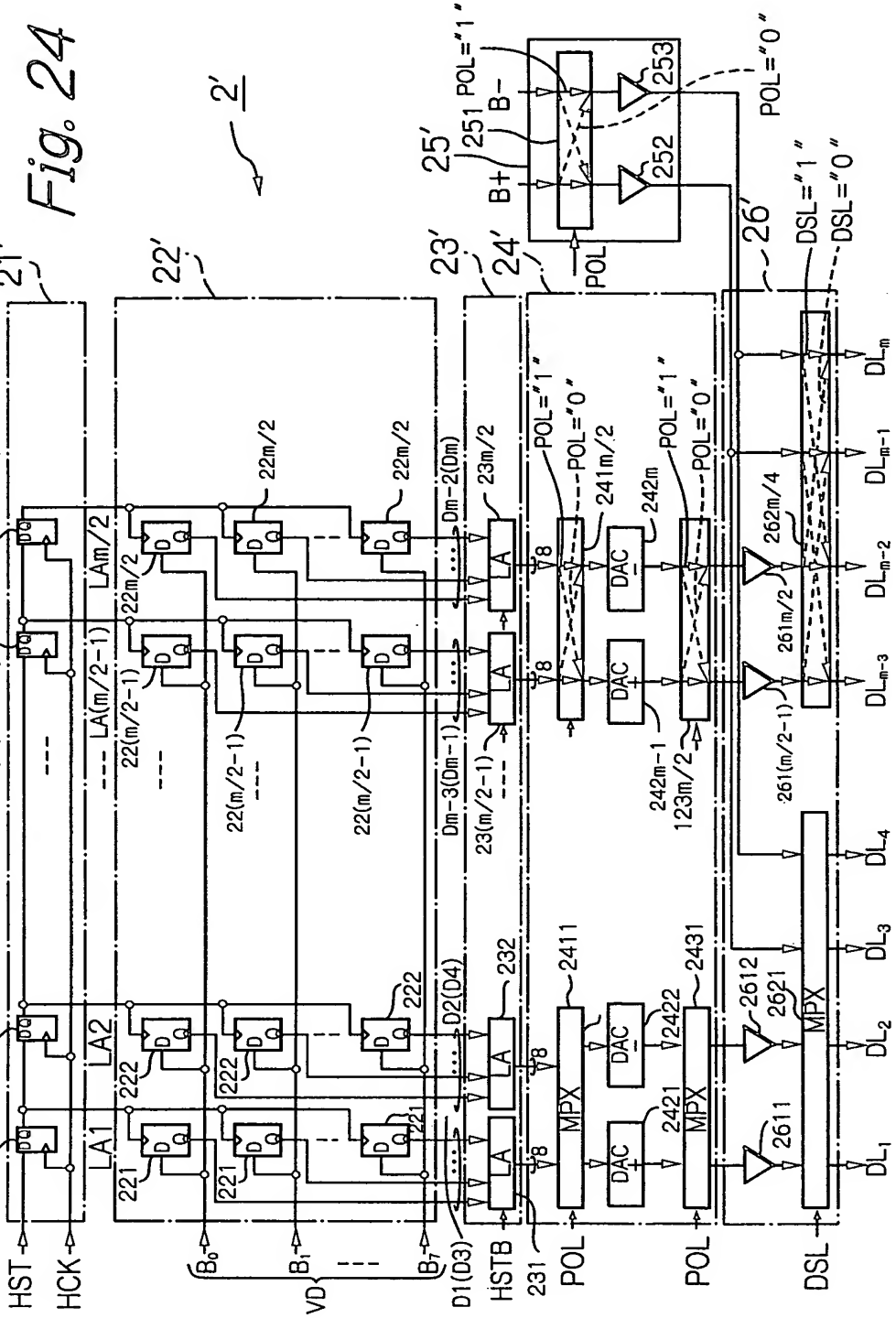

2'
21'
22'
23'
24'
25'
26'
HST
HCK
VD
HSTB
POL
DSL
B+
B-
LA1
LA2
LAm/2
LA(m/2-1)
211
212
21m/2
21(m/2-1)
221
222
22m/2
22(m/2-1)
231
232
LA
MPX
DAC
2411
2421
2431
2422
2611
2612
2621
241m/2
242m
242m-1
123m/2
251
252
253
261m/2
262m/4
261(m/2-1)
POL="1"
POL="0"
DSL="1"
DSL="0"
D1(D3)
D2(D4)
Dm-3(Dm-1)
Dm-2(Dm)
23m/2
23(m/2-1)
DL1
DL2
DL3
DL4
DLm-3
DLm-2
DLm-1
DLm

Fig. 25

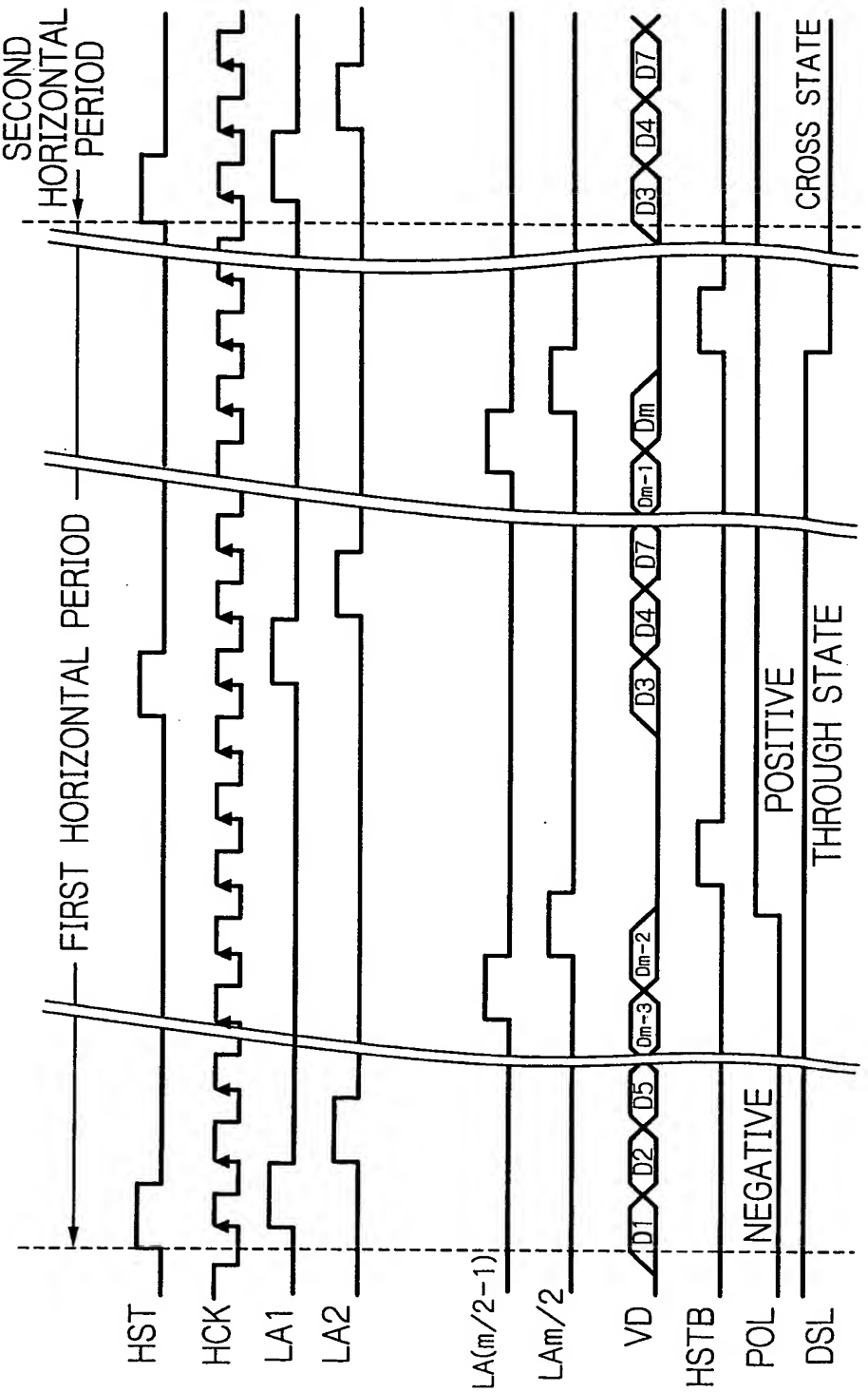

SECOND HORIZONTAL PERIOD
FIRST HORIZONTAL PERIOD
HST
HCK
LA1
LA2
LA(m/2-1)
LAm/2
VD
HSTB
POL
DSL
D1
D2
D5
Dm-3
Dm-2
D3
D4
D7
Dm-1
Dm
NEGATIVE
POSITIVE
CROSS STATE
THROUGH STATE

Fig. 26

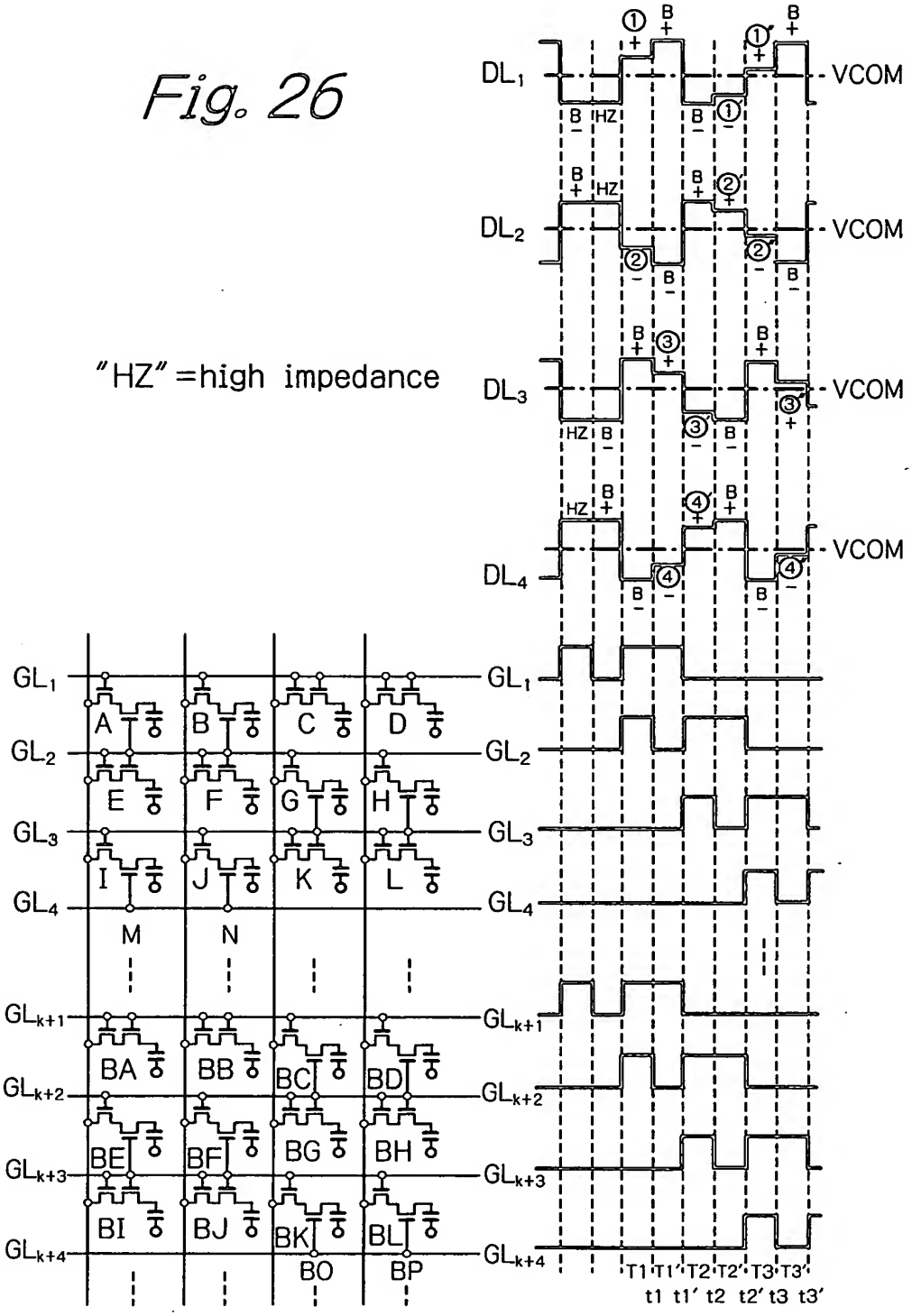
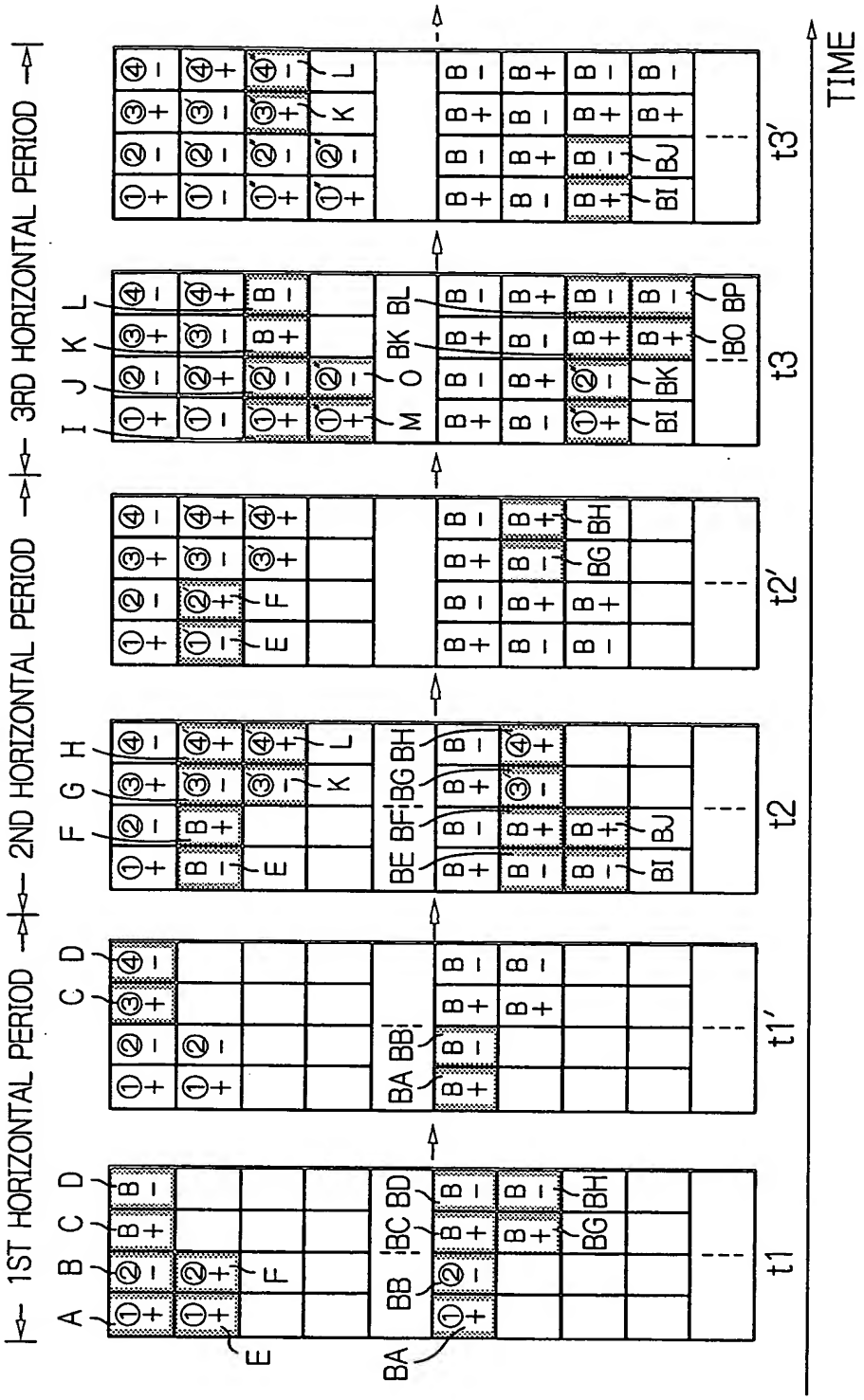

"HZ"=high impedance
DL1
DL2
DL3
DL4
VCOM
GL1
GL2
GL3
GL4
GLk+1
GLk+2
GLk+3
GLk+4
A
B
C
D
E
F
G
H
I
J
K
L
M
N
BA
BB
BC
BD
BE
BF
BG
BH
BI
BJ
BK
BL
BO
BP
T1 T1' T2 T2' T3 T3'
t1 t1' t2 t2' t3 t3'

Fig. 27


1ST HORIZONTAL PERIOD
2ND HORIZONTAL PERIOD
3RD HORIZONTAL PERIOD
A B C D
F G H
I J K L
t1
t1'
t2
t2'
t3
t3'
TIME